IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Michael B. Galles, et al.
Serial No.:	10/696,146
Filing Date:	October 29, 2003
Confirmation No.:	5506
Group Art Unit:	2181
Examiner:	William M. Treat
Title:	MULTI-PROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REQUEST FOR PRE-APPEAL BRIEF REVIEW

In response to the Advisory Action mailed October 19, 2006, Applicant respectfully requests a Pre-Appeal Brief review of this Application so that the rejection of the claims and the objections to the Application can be reconsidered prior to submission of an Appeal Brief.

REMARKS

This Request for Pre-Appeal Brief Review is being filed in accordance with the provisions set forth in the Official Gazette Notices of July 12, 2005 and January 10, 2006. Pursuant to the Official Gazette Notices, this Request for Pre-Appeal Brief Review is being filed concurrently with a Notice of Appeal. Applicant respectfully requests reconsideration of the Application in light of the remarks set forth below.

In the prosecution of the present Application, the Examiner's rejections, objections, and assertions contain clear errors of law, including a failure to establish a prima facie case of anticipation and obviousness. To assist the Panel in the review of this Request for Pre-Appeal Brief Review, Applicant submits the following brief summary for consideration.

With respect to the §112 rejections, support for the central processing unit having an integrated memory controller is clearly provided in FIGURE 2. FIGURE 2 clearly shows a central processor 20 having a memory controller 30 and a memory directory 18 therein integrated, along with memory 16, into the single device of processor 12. Memory controller 30 and memory directory 18 are clearly shown to be within central processing unit 20. Applicant's specification at page 7, lines 5-7, particularly discloses that these components are integrated with memory 16 into a single device, processor 12. Thus, the specification provides clear support for the claim language.

With respect to the Kabemoto, et al. patent, Independent Claim 1 recites ". . . each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a

plurality of memory references to data within the integrated memory . . ." By contrast, the Kabemoto, et al. patent shows processor and cache units separate from each other and a separate memory control module. Moreover, a directory memory is disclosed as being separate and apart from the processor. The Examiner seems to refer to processor element 14-1 of the Kabemoto, et al. patent in stating that each component of the claimed invention is found therein but has not shown how the processor 16-1 itself includes each component of the processor of the claimed invention. The processor element 14-1 of the Kabemoto, et al. patent includes a processor 16-1, a cache unit 18-1, and a snoop unit 20-1. The Examiner shows that the processor 16-1 of the Kabemoto, et al. patent includes a memory 36 and 38 but readily admits that a memory controller 35 and a memory directory 40 of the Kabemoto, et al. patent are not included in its processor 16-1 by showing that the memory controller 35 and the memory directory 40 are in the cache unit 18-1 which is separate and apart from the processor 16-1. As a result, the processor of the Kabemoto, et al. patent does not include the resources and functionality of the processor in the claimed invention and the Examiner has not provided any teaching within the Kabemoto, et al. patent to support the rejection of the claims.

With respect to the Chase, et al. patent, Independent Claim 1 recites ". . . each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory . . ." By contrast, the station 12 of the Chase, et al. patent equated by the Examiner as the claimed processor shows a processor 18 and a storage 21 with a cache 20 separate and apart from its processor 18. Thus, the storage 21 and

cache 20 of the Chase, et al. patent are not integrated within its processor 18 as would be required by the claimed invention. In addition, the Chase, et al. patent expressly discloses a cache directory 16 in a directory server 17 that is separate and apart from station 12 and its processor 18 and storage 21. The Chase, et al. patent clearly discloses the use of a cache directory 16 in a server 17 separate and remote from any of its stations 12 for use with cache 20 within station 12. The Chase, et al. patent clearly teaches away from any use of a directory within its station 12 and being integrated with its processor 18 let alone being integrated within a central processing unit as required by the claimed invention. In fact, the memory directory 16 is disclosed in the Chase, et al. patent as also being separate from a processor 18 within its directory server 17. Further, the Chase, et al. patent provides no mention of a memory controller within station 12 or processor 18 let alone any integration of a memory controller within its processor 18. The Chase, et al. patent teaches away from this integration by having all of the claimed elements in separate devices. The processor of the Chase, et al. patent does not include the resources and functionality of the processor or the central processing unit provided in the claimed invention. As a result, the Examiner has not provided any teaching within the Chase, et al. patent to support the rejection of the claims.

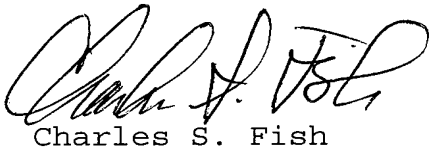
With respect to the added subject matter objection, amendments were made to the specification consistent with the depiction in FIGURE 2 of central processing unit 20 in addressing the Examiner's objections to the drawings under 37 C.F.R. §1.84(p)(5). Thus, no new matter has been added to the specification.

CONCLUSION

Applicant has now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other apparent reasons, Applicant respectfully requests allowance of all pending claims.

The Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
BAKER BOTTS L.L.P.
Attorneys for Applicant



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November 9, 2006

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